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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/855,641

05/15/2001

Jeremy E. San

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27562

7590

12/05/2007

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EXAMINER

LIANG, REGINA

ART UNIT

PAPER NUMBER

2629

MAIL DATE

DELIVERY MODE

12/05/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 09/855,641	Applicant(s) SAN ET AL.	
	Examiner Regina Liang	Art Unit 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 135-140, 142-153, 186-191, 195-201, 204 and 205 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 135-140, 142-153, 186-191 and 195-201, 204, 205 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/07 has been entered. Claims 135-140, 142-153, 186-191, 195-201, 204, 205 are pending in the application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 135-140, 142-153, 186-191, 195-201, 204, 205 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not provide support for "said special purpose hardware graphics processor unit performs a 3x3 matrix transformation of x, y and z graphics data points to provide

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rotated and/or scaled polygon-based 3D objects at high speed” as is now claimed in independent claims 135 186 and 187, 204. All dependent claims are rejected for the same reason.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 135-140, 142-153, 186-191, 195-201, 204, 205 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-57 of U.S. Patent No. 5,388,841 in view of Logg (US 5,415,549).

The following is the example for comparing claim 135 of this application and claim 43 of US 5,388,841.

Claim 135 of this application	claim 43 of US 5,388,841
a home video game system for use with a	a video game system for use with a television

television type monitor display device, comprising:	type display comprising:
a game program processing unit for executing at least a portion of a videographics game program that includes instructions for drawing one or more polygons for constructing and displaying 3D objects; and a video RAM for providing video frame data to a display device; and	a game microprocessor for executing instructions of a video game program, and a picture processing unit coupled to said game microprocessor for performing picture processing tasks under the control of said game microprocessor; a program memory for storing said video game program; and
a programmable special purpose hardware graphics processor unit connected to the game program processing unit for receiving information relating to one or more polygons for constructing and displaying 3D graphic objects, the special purpose hardware graphics processor programmed to process pixel data for subsequent transfer to said video RAM corresponding to one or more portions of polygon-based 3D objects to be displayed,	A programmable graphics processor coupled to said program memory and connected in used to said game microprocessor for executing at least some of said video game program instructions; said game microprocessor and picture processing unit are embodied in a video game system main processing unit and said program memory and graphics processor are embodied within a video game cartridge.

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where said special purpose hardware graphics processor unit performs a 3x3 matrix transformation of x, y and z graphics data points to provide rotated and/or scale polygon-based 3D objects at high speed.	
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From the comparison above, claim 43 of US 5,388,841 differs from claim 135 of this application in not having instructions for drawing one or more polygons for displaying 3D objects and the graphics processor not performs a 3x3 matrix transformation of x, y and z graphics data points to provide rotated and/or scale polygon-based 3D objects at high speed. However, Logg is cited to teach a game device which uses polygon graphics to simulate 3D images (col. 2, lines 10-14), and Logg also teaches a graphics processor performing matrix transformation of graphics data points to provide rotated and/or scaled polygon-based 3D objects at high speed (col. 10, lines 45-62 for example). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify **the game microprocessor and the graphics processor unit** in claim 43 of US 5,388,841 to have the features as taught by Logg to so as to simulate 3D images in the video game device.

Claim Rejections - 35 USC § 103

7. Claims 135, 136 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loffredo (US 5,016,876) in view of Logg.

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As to claim 135, Fig. 1 of Loffredo discloses a home video game system for use with a television type monitor display device, comprising: a game program processing unit (digital computer 22, col. 4, line 53 to col. 5, line 2, col. 5, lines 54-56) for executing at least a portion of a videographics game program that includes instructions for displaying objects; a video RAM (34) for providing video frame data to a display device; and a programmable graphics processor unit (coprocessor 130) connected to the game program processing unit for receiving information relating graphic objects for constructing and display graphic objects from the game program processing unit, the programmable graphics processor programmed to process pixel data for subsequent transfer to the video RAM for constructing the objects for display on the television type monitor display (col. 9, line 23 to col. 10, line 2).

Loffredo does not explicitly disclose the instructions for drawing one or more polygons for displaying 3D objects and the graphic processor unit performing matrix transformation of x, y and z graphics data points to provide rotated and/or scaled polygon-based 3D objects at high speed. However, Loffredo teaches his video game device having the capability to create a composite scene by overlaying successive planes image data so as to allow a real-time animation of composite scenes. Logg teaches a game device have used polygon graphics to simulate 3D images (col. 2, lines 10-14); Logg also teaches a graphics processor performing matrix transformation of graphics data points to provide rotated and/or scaled polygon-based 3D objects at high speed (col. 10, lines 45-62 for example). Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the game device of Loffredo to have the features as taught by Logg so as to simulate 3D images in a real-time animation in the video game device of Loffredo.

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As to claim 136, Loffredo teaches the programmable graphics processor (130) is a coprocessor.

8. Claims 137-140, 142-153, 186-201, 204, 205 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loffredo and Logg as applied to claim 135 above, and further in view of "PC TECH JOURNAL, "Custom-Tailored Graphics: TMS 34010, by Ed McNierney; hereafter McNierney).

The combination of Loffredo with Logg teaches the claimed invention, but does not disclose the internal architecture of the processor. However, McNierney discloses the internal architecture of the processor that includes a coprocessor that has a high-speed arithmetic logic unit and programmable instruction cache that allows it to fetch instructions in parallel with executing instructions and accessing registers and local memory. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the graphic processor of Loffredo as modified by Logg to have the internal architecture as taught by McNierney for faster data access processing.

As to claims 137, 139-140, 142-152, 189-191, 195-201, McNierney discloses in page 68 last column last paragraph Tms34010 that is a pipelined processor and includes an Arithmetic Logic Unit, barrel shifter (multiplier unit that performs multiply operation using at least 16-bit length, a cache RAM and plurality of registers and also is capable of performing graphics-intensive tasks like rotation or scaling of polygon based objects. In addition the TMS34010 include the pixel plotting circuit (page 68-70), and it includes a set of instructions (page 71) an instruction for texture mapping and an instruction for controlling transparency of display object

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and an instruction for fractional signed multiply instruction are included in the set (page 73).

McNierney also discloses in page 71 that graphics processor incorporates an arithmetic Logic Unit, cache RAM, high speed multiplier and plurality of register fabricated on a single chip.

As to claims 153, 187, Loffredo does not disclose a CD ROM reader device. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memory storage of Loffredo to have a CD ROM to improve the video game by permitting a different game memory with instructions and data for a different game to be substituted.

As to claim 188, Loffredo teaches the programmable graphics processor (130) is a coprocessor.

As to claim 138, 205, Loffredo discloses in col. 3, lines 24-27 DMA transfer of pixel data to video RAM.

As to claims 186, 204, the combination of Loffredo with Logg teaches the claimed invention as discussed in claim 135 above. Furthermore, McNierney discloses in page 70 the first and second column computing display screen position coordinates for the rotate/or scaled polygon-based object; further Loffredo teaches in col. 5, line 54 to col. 6, line 25 writing pixel color information corresponding to the rotated/or scaled polygon-based object to the video RAM.

Response to Arguments

9. Applicant's arguments filed 10/31/07 have been fully considered but they are not persuasive.

Applicant's remarks regarding the double patenting rejection on page 12 are not persuasive since the feature of "special purpose hardware graphics processor that performs 3x3

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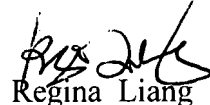
matrix transformations on x, y and z graphics data to provide rotated and scaled polygon-based 3D object” is taught by Logg, see the rejection above.

Applicant’s remarks Loffredo and Logg on pages 12-15 are not persuasive. Logg teaches a game device having a program which has used polygon graphics to simulate 3D images, and Logg also teaches the “graphics processor that performs 3x3 matrix transformations on x, y and z graphics data to provide rotated and scaled polygon-based 3D object” (col. 10, lines 45-62 for example). Therefore, the combination of Loffredo and Logg renders the claims obvious.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Regina Liang
Primary Examiner
Art Unit 2674

12/4/07